

# Irradiation induced effects in the FE-I4 front-end chip of the ATLAS IBL detector

Alessandro La Rosa  
on behalf of ATLAS collaboration

**Abstract**—The ATLAS Insertable B-Layer (IBL) detector was installed into the ATLAS experiment in 2014 and has been in operation since 2015. During the first year of IBL data taking an increase of the low voltage currents associated with the FE-I4 front-end chip was observed and this increase was traced back to the radiation damage in the chip. The dependence of the current on the total-ionising dose and temperature has been tested with X-ray and proton irradiations and will be presented in this paper together with the detector operation guidelines.

## I. INTRODUCTION

ATLAS [1] is a general-purpose experiment operating at the Large Hadron Collider (LHC) at CERN. The ATLAS detector was designed to be sensitive to a wide range of physics signatures to fully exploit the physics potential of the LHC at a nominal luminosity of  $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . As most of the final states of collisions in the ATLAS experiment include charged particles, an excellent tracking system is essential.

The ATLAS Insertable B-Layer (IBL) [2] is the innermost layer of the ATLAS pixel detector [3]. It is one of the major upgrades to the ATLAS experiment carried out during the long shutdown of the LHC in 2013–2014.

The IBL detector is the additional fourth pixel layer that was built around the new beryllium beam pipe and then inserted inside the Pixel detector in the core of the ATLAS detector. It consists of 14 carbon fibre staves instrumented along 64 cm, 2 cm wide, and tilted in  $\phi$  by  $14^\circ$  surrounding the beam-pipe at a mean radius of 33 mm from the beam axis and providing a pseudo-rapidity coverage of  $\pm 3$ . Each staff, with integrated  $\text{CO}_2$  cooling, is equipped with 32 front-end chips (FE-I4 [4]) bump bonded to silicon sensors.

The FE-I4 chip is designed in 130 nm CMOS technology which features an array of  $80 \times 336$  pixels with a pixel size of  $50 \times 250 \mu\text{m}^2$ . Each pixel contains an independent, free running amplification stage with adjustable shaping, followed by a discriminator with independently adjustable threshold. The FE-I4 keeps track of the time-over-threshold (ToT) of each discriminator with 4-bit resolution, in counts of an external supplied clock of 40 MHz frequency. The FE-I4 operates by feeding the common power supply to analog signal amplifiers and digital signal-process circuits, referred to as the low-voltage (LV) power supply and the clock input.

The IBL detector is designed to be operational until the end of the LHC Run 3, where the total integrated luminosity is expected to reach  $300 \text{ fb}^{-1}$ . The detector components are qualified to work up to 250 Mrad of total ionising dose (TID).

Alessandro La Rosa is with the Max-Planck-Institut für Physik (Werner-Heisenberg-Institut), Föhringer Ring 6, D-80805 München, Germany (telephone: +41-22-76-63600, e-mail: alessandro.larosa@cern.ch).

During the first year of the IBL operation in 2015 a significant increase of the LV current of the front-end chip and the detuning of its parameters (threshold and time-over-threshold) have been observed in relation to the received TID. In this paper, the TID effects in the FE-I4 chip are reported based on studies performed in the laboratory using X-ray and proton irradiation sources for various temperature and irradiation intensity conditions. Based on these results, an operation guideline of the IBL detector is presented.

## II. OBSERVATIONS

During the operation of the IBL detector, the LV current of the FE-I4 chip was stable at a value of 1.6–1.7 A (for a four-chip unit) until the middle of September 2015. Then, the current started to rise up significantly (see Figure 1), and the change of the current during September to November 2015 was more than 0.2 A even within a single LHC fill, depending on the luminosity and the duration of the fill.

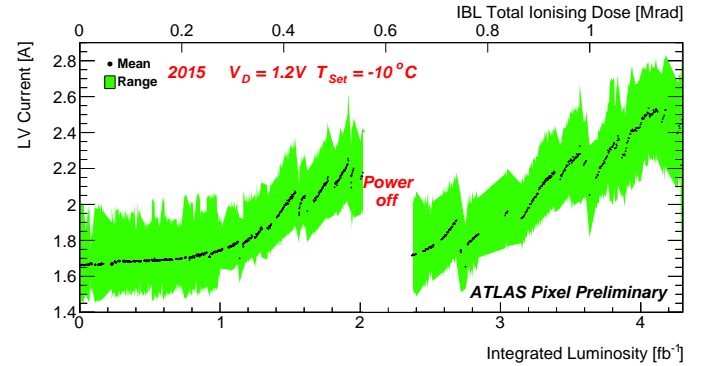


Fig. 1. Mean low voltage (LV) current in IBL FE-I4 chips during stable beam as a function of integrated luminosity and total ionising dose (TID). In the period from September to November 2015 the IBL detector was switched off during one LHC fill (due to safety concerns in early October 2015). The mean LV currents are averaged for all modules across 100 luminosity blocks and there is no obvious dependence of LV current on module group position. The TID is calculated from integrated luminosity [5].

With the increase of the LV current, the temperature of IBL modules also changes (Figure 2). The change of the thermo-mechanical condition of the IBL resulted in the change of the IBL distortion magnitude, and a clear relation between the module temperature and the distortion magnitude was observed [6].

In addition, as shown for example in Figure 3, the calibration of the FE-I4 chips for the analog discriminator threshold and the target ToT were observed to drift rapidly despite frequent updating of the calibration.

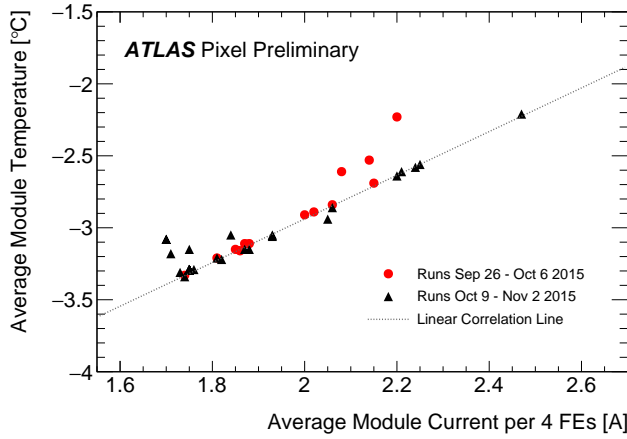


Fig. 2. Performance of the IBL modules during high luminosity proton-proton collision runs from September to November 2015, separated into the periods before (red circles) and after (black triangles) the long power-off on October 6. The data are displayed as a function of the average module current per 4 front-ends of the IBL and compared to a linear dependence. The average module temperature is shown [7].

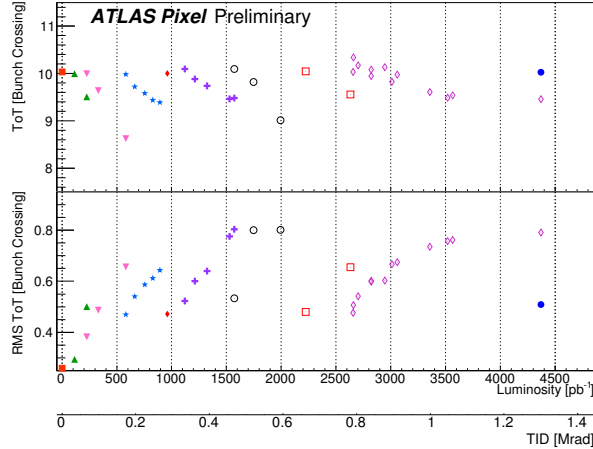


Fig. 3. The time-over-threshold (ToT) and its RMS as a function of the integrated luminosity or total ionising dose (TID) [8]. The detector was regularly retuned, and each marker type corresponds to a single tuning of the detector.

### III. IRRADIATION TEST-RESULTS

The increase of the LV current of the FE-I4 chip and the drifting of its tuning parameters were traced back to the generation of a leakage current in NMOS transistors induced by radiation higher than usual. The radiation induces positive charges that are quickly trapped into the shallow-trench-insolation (STI) oxide at the edge of the transistor. Their accumulation builds up an electric field sufficient to open a source-drain channel where the leakage current flows. If the accumulation of positive charges is relatively fast, the formation of interface states is a slower process. The negative charges trapped into interface states start to compete with the oxide-trapped charges with a delay. This is what gives origin to the so called rebound effect [9]. Dedicated laboratory measurements [10] of irradiated single transistors in 130 nm CMOS commercial technologies showed that the increase of

the leakage current reaches its peak value between 1 Mrad and 3 Mrad. For higher TID the current decreases to a value close to the pre-irradiated one.

To reproduce and analyse the effects described above during the FE-I4 chip operation, several irradiations and electrical tests were performed by using X-ray (Seifert RP149 [11], and XRAD-iR-160 [12]) and proton (Bern Cyclotron [13]) sources. Since the current increase in NMOS transistors depends on dose rate and temperature [9], measurements under different temperature and dose rate conditions have been carried out to qualify this dependency.

The first irradiation test aimed at measuring the boundary current (at a given temperature and dose rate) that the chip always approaches after annealing periods and re-irradiation. Figure 4 shows the increase of the current consumption of a single FE-I4 chip in data taking condition as a function of the TID. The temperature of the chip was 38 °C and the dose rate 120 krad h<sup>-1</sup>. After reaching the maximum of each peak the chip was annealed for several hours resulting in the observed partial recovery.

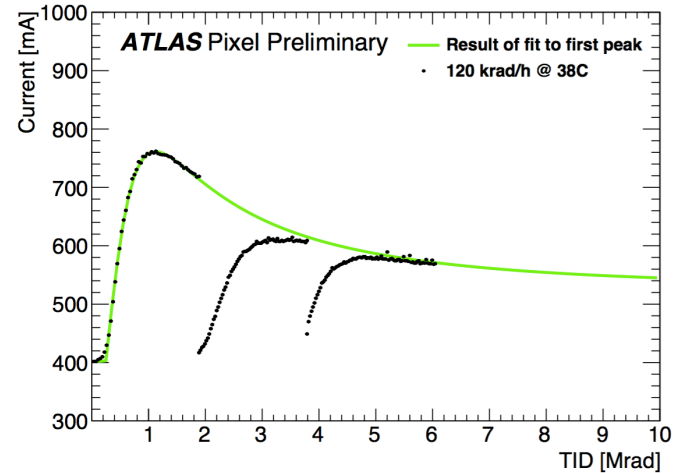


Fig. 4. Increase of the current consumption of a single FE-I4 chip in data taking condition as a function of the total ionising dose (TID). The temperature of the chip was 38 °C and the dose rate 120 krad h<sup>-1</sup>. After reaching the maximum of each peak the chip was annealed several hours resulting in the observed partial recovery [15]. The fit performed on the first set of data (first peak) has been carried out by using the current parametrisation described in Ref. [14].

Then, to study the dependence of the LV current increase on temperature and dose rate several irradiation tests were performed by setting one of those variables and changing the other. Figure 5 shows the results of three different measurements, performed with three different and previously not irradiated chips. The dose rate was 120 krad h<sup>-1</sup> and the temperatures were 38 °C, 15 °C and -38 °C. Before irradiation the LV current of the three chips was 400 mA (38 °C), 360 mA (15 °C) and 380 mA (-38 °C). For comparison Figure 6 shows the result of two different measurements where the temperature was kept fix at 15 °C, while the dose rate set to 120 krad h<sup>-1</sup> or 420 krad h<sup>-1</sup>. Also in this case the tests were performed with different and previously not irradiated chips.

The measurements described above revealed two facts: i) at a given dose rate the LV current increase is stronger at

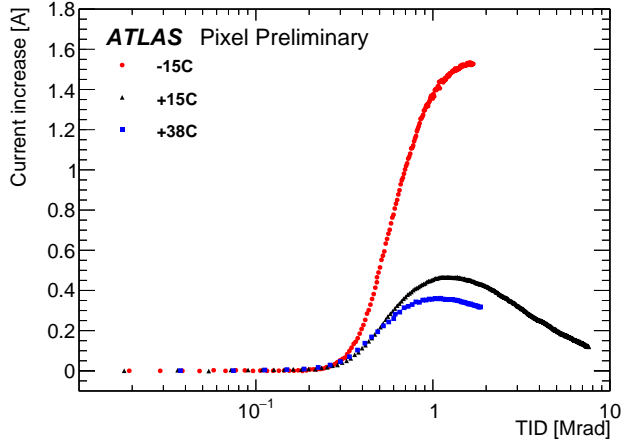


Fig. 5. Increase of the LV current of three single FE-I4 chips in data taking condition as a function of the total ionising dose (TID) in logarithmic x-axis scale. Test measurements were carried out at 38 °C (blue points), at 15 °C (black points) and at  $-15^{\circ}\text{C}$  (red points) with a dose rate of  $120\text{ krad h}^{-1}$ . A dose rate up to  $10\text{ krad h}^{-1}$  is expected in the experiment. The LV current of the single FE-I4 chips before irradiation were 400 mA (38 °C), 360 mA (15 °C) and 380 mA ( $-38^{\circ}\text{C}$ ) [15].

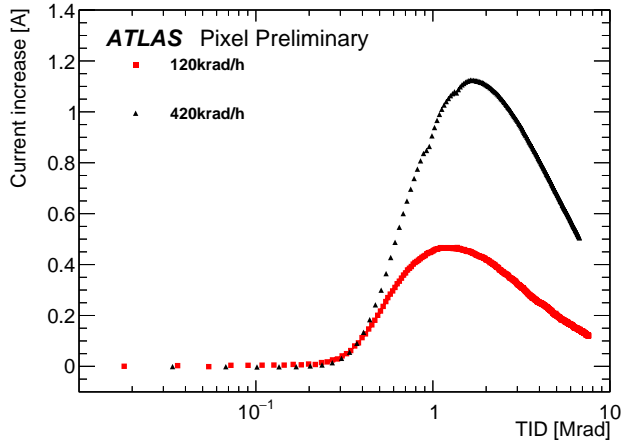


Fig. 6. Increase of the LV current of two single FE-I4 chips in data taking condition as a function of the total ionising dose (TID) in logarithmic x-axis scale. Test measurements were carried out at 15 °C with a dose rate of  $120\text{ krad h}^{-1}$  (red points) and  $420\text{ krad h}^{-1}$  (black points). A dose rate up to  $10\text{ krad h}^{-1}$  is expected in the experiment. The LV current of the single FE-I4 chips before irradiation were 380 mA ( $420\text{ krad h}^{-1}$ ) and 360 mA ( $120\text{ krad h}^{-1}$ ) [15].

lower temperatures; ii) at a given temperature, the LV current increase is stronger at higher dose rates.

To simulate the dose rate conditions of the 2015 and 2016 data taking, a first irradiation was performed at  $-15^{\circ}\text{C}$  and  $120\text{ krad h}^{-1}$ . This was followed by several hours of annealing and a second irradiation this time performed at  $5^{\circ}\text{C}$  and  $420\text{ krad h}^{-1}$ . As shown in Figure 7 the second LV current peak is lower than the first one, i.e. by increasing the operational temperature of the chip it was possible to keep the increase of the LV current below the boundary current given by the first irradiation.

To verify that a temperature of  $5^{\circ}\text{C}$  is safe for the IBL

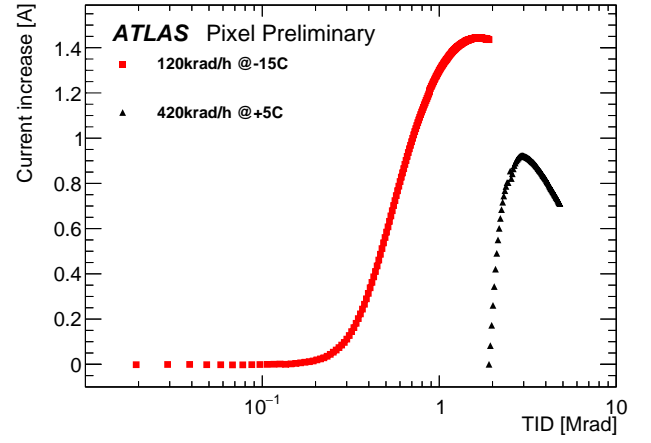


Fig. 7. Increase of the LV current of a single FE-I4 chip in data taking condition as a function of the total ionising dose (TID) in logarithmic x-axis scale during two consecutive irradiation campaigns in a lab measurement. Between the two irradiations several hours of annealing period at room temperature was performed, and resulted in the observed recovery. The TID of both irradiations is summed up. The LV current of a single FE-I4 chip before irradiation was 380 mA (first step) and 550 mA (second step) [15].

detector operation, a measurement at  $10\text{ krad h}^{-1}$  was performed. The maximum LV current increase was of the order of 250 mA, which gives a LV current increase of 1 A for a four-chip unit, which would not exceed the safety limit of the LV current originally set to 2.8 A.

In principle, lower operational temperatures are favourable for the sensor performance and properties after irradiation and therefore preferred. Consequently, irradiation and electrical tests were also performed at a temperature of  $0^{\circ}\text{C}$  to investigate the feasibility for a colder operation. In addition investigated was the evolution of the maximum of the LV current peak under several irradiation steps followed, interleaved with periods of annealing. In this case the first two consecutive peaks of the LV current increase exceeded the maximum current allowed for a safe detector operation. Therefore, it was decided to set  $5^{\circ}\text{C}$  as minimum temperature for a safe and successful data taking.

#### IV. DETECTOR OPERATION GUIDELINE

Based on the observations during the first year of data-taking in 2015 with the IBL detector, it was decided to raise the safety limit for the IBL LV currents from 2.8 A to 3 A for module groups of four chips, which means a current consumption of 750 mA per chip. Since the average current consumption for a single FE-I4 chip is about 400 mA before irradiation, the increase of the current due to the TID effects can not be higher than 350 mA per chip.

Given the above results it was decided to increase the IBL operation temperature from  $-10^{\circ}\text{C}$  to  $15^{\circ}\text{C}$ . In addition, the digital supply voltage ( $V_D$ ) was lowered from 1.2 V to 1 V to decrease the LV current.

Thanks to dedicated measurements at  $5^{\circ}\text{C}$  and at a dose rate comparable to the LHC in 2016 ( $10\text{ krad h}^{-1}$ ), it is proven that the current increase is of the order of 250 mA. With this a

module group of four chips does not exceed the safety limit of 3 A. Therefore operating the IBL detector at 5 °C is safe with respect to the expected luminosity in 2016. The temperature of the IBL cooling system was lowered to a set point of 5 °C. The digital supply voltage ( $V_D$ ) was raised from 1 V to 1.2 V, after an accumulated dose of  $\sim 5$  Mrad which, as the measurements show, is well beyond the high peak region for the current consumption.

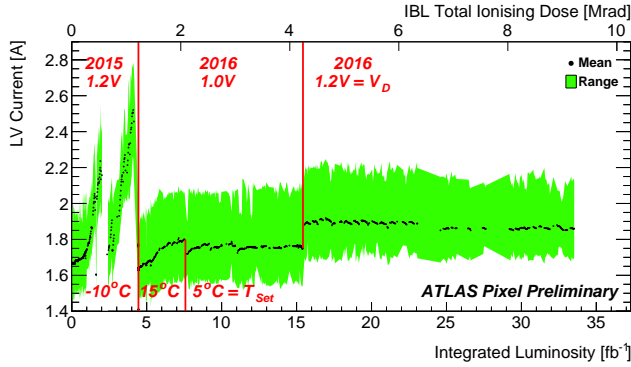


Fig. 8. Mean Low Voltage (LV) current in IBL FE-I4 chips during stable beam against integrated luminosity and total ionising dose (TID); values are averaged for all modules across 100 luminosity blocks. Changes in digital voltage ( $V_D$ ) are highlighted. The set temperatures ( $T_{Set}$ ) of the modules correspond to actual module temperatures of about -5°C, 20°C and 10°C. There were significant increases in LV current during 2015; this was addressed in 2016 by increasing the module temperatures and decreasing the digital voltage. The digital voltages were later increased back to decrease readout error frequency [5].

An overview of the mean LV current of the IBL FE-I4 chips as a function of integrated luminosity and TID during stable beam is shown in Figure 8. The LV currents are averaged for all modules across 100 luminosity blocks, and the changes in digital supply voltage ( $V_D$ ) and the temperature ( $T_{Set}$ ) are highlighted.

In addition, since the shift of the tuning parameters can be seen even at low dose rates and warmer temperatures, a retuning on a regular basis was performed.

## V. SUMMARY

The Insertable B-Layer (IBL) is the innermost pixel barrel layer of the ATLAS detector installed in 2014.

During the first year of data taking in 2015, a peculiar increase of the LV current of the front-end chip and the detuning of its parameters (threshold and time-over-threshold) have been observed in relation to received total ionising dose. It was tracked back to the generation of a leakage current in NMOS transistors induced by radiation.

Dedicated irradiation and electrical tests of FE-I4 chips showed that the leakage current reaches its peak value when the total ionising dose is in the range of 1 Mrad – 3 Mrad, and above this the current decreases to a value close to the pre-irradiation one. This effect was shown to be temperature and dose rate dependent.

Thanks to intensive studies it was possible to apply special detector settings to still guarantee a successful data-taking.

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